WHAT IS CLAIMED IS:

1. A method for avoiding oxide gouging in shallow trench isolation (STI) regions of a semiconductor device comprising the steps of:

etching a trench in an STI region;

depositing an insulating material in said trench;

forming a gate oxide layer overlying said STI region and extending beyond the boundaries of said STI region;

depositing a polysilicon layer over said gate oxide layer;

depositing an anti-reflective coating (ARC) layer over said polysilicon layer;

etching a portion of said ARC layer over said STI region leaving a remaining portion of said ARC layer over said STI region and extending beyond the boundaries of said STI region;

etching an exposed portion of said polysilicon layer and said gate oxide layer over said STI region leaving a remaining portion of said polysilicon layer and said gate oxide layer over said STI region and extending beyond the boundaries of said STI region;

depositing a protective cap over said STI region and extending beyond the boundaries of said STI region, wherein said protective cap covers said remaining portion of said ARC layer over said STI region and covers said insulating material over said STI region;

etching a portion of said protective cap to expose said remaining portion of said ARC layer while maintaining protection of said insulating material; and

etching said remaining portion of said ARC layer;

wherein said insulating material is protected during etching of said remaining portion of said ARC layer by said protective cap.

2. The method as recited in claim 1, wherein said protective cap comprises photoresist material.

3. The method as recited in claim 2, wherein said photoresist material has a thickness of about 800Å to 1200Å.

4. The method as recited in claim 1, wherein said remaining portion of said ARC layer is etched using a plasma etch process.

5. The method as recited in claim 1, wherein said insulating material comprises thermal oxide.

6. A device, comprising:

a trench in an STI region;

insulating material filled in said trench;

a gate oxide layer covering a portion of said STI region and extending beyond the boundaries of said STI region;

a polysilicon layer covering said gate oxide layer, wherein said polysilicon layer covers said portion of said STI region and extends beyond the boundaries of said STI region;

an anti-reflective coating (ARC) layer covering said polysilicon layer, wherein said ARC layer covers said portion of said STI region and extends beyond the boundaries of said STI region; and

a protective cap covering said STI region and extending beyond the boundaries of said STI region, wherein said protective cap covers said ARC layer covering said portion of said STI region, wherein said protective cap covers said insulating material filled in said trench over said STI region.

7. The system as recited in claim 6, wherein said protective cap comprises photoresist material.

8. The system as recited in claim 7, wherein said photoresist material has a thickness of about 800Å to 1200Å.

9. The system as recited in claim 6, wherein said insulating material comprises thermal oxide.

10. A method for avoiding oxide gouging in shallow trench isolation (STI) regions of a semiconductor device comprising the steps of:

etching a trench in an STI region;

depositing an insulating material in said trench;

depositing an anti-reflective coating (ARC) layer over said STI region and extending beyond the boundaries of said STI region;

etching a portion of said ARC layer over said STI region leaving a remaining portion of said ARC layer over said STI region and extending beyond the boundaries of said STI region; and

depositing a protective cap covering said STI region and extending beyond the boundaries of said STI region, wherein said protective cap covers said remaining portion of said ARC layer and said insulating material over said STI region.

11. The method as recited in claim 10 further comprising the steps of:

etching a portion of said protective cap to expose said remaining portion of said ARC layer while maintaining protection of said insulating material; and

etching said remaining portion of said ARC layer;

wherein said insulating material is protected during etching of said remaining portion of said ARC layer by said protective cap.

12. The method as recited in claim 10, wherein said protective cap comprises photoresist material.

13. The method as recited in claim 12, wherein said photoresist material has a thickness of about 800Å to 1200Å.

14. The method as recited in claim 11, wherein said remaining portion of said ARC layer is etched using a plasma etch process.

15. The method as recited in claim 10, wherein said insulating material comprises thermal oxide.